

CLAIMS

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1 1. A semiconductor structure containing a field oxide, comprising:
2 a semiconductor substrate including an isolation region and an active region;
3 a field oxide formed on the semiconductor substrate in the isolation region;
4 a first pad layer formed on the semiconductor substrate in the active region;
5 a second pad layer formed on the semiconductor substrate not covered by the
6 first pad layer, wherein the second pad layer has a smaller thickness than the first pad
7 layer;
8 a mask layer formed on the first pad layer, wherein the mask layer has a larger
9 width than the first pad layer to form a cavity beneath the mask layer and next to the
10 first pad layer; and
11 a mask filler filled in the cavity.

1 2. The semiconductor structure as claimed in claim 1, wherein the first pad
2 layer is an oxide.

1 3. The semiconductor structure as claimed in claim 1, wherein the second pad
2 layer is an oxide.

1 4. The semiconductor structure as claimed in claim 1, wherein the first pad
2 layer has a thickness of 100 Å to 250 Å.

1 5. The semiconductor structure as claimed in claim 1, wherein the second pad
2 layer has a thickness of 60 Å to 120 Å.

1 6. The semiconductor structure as claimed in claim 1, wherein the mask layer
2 is a nitride.

1 7. The semiconductor structure as claimed in claim 1, wherein the mask filler
2 is a nitride.

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1 8. The semiconductor structure as claimed in claim 1, wherein the cavity is
2 indented from the sidewall of the mask layer by 300 Å to 700 Å.

1 9. A semiconductor structure containing a field oxide, comprising:
2 a semiconductor substrate including an isolation region and an active region;
3 a field oxide formed on the semiconductor substrate in the isolation region;
4 a first pad layer formed on the semiconductor substrate in the active region;
5 a second pad layer formed on the semiconductor substrate not covered by the
6 first pad layer, wherein the second pad layer has a smaller thickness than the first pad
7 layer;
8 a mask layer formed on the first pad layer, wherein the mask layer has a larger
9 width than the first pad layer to form a cavity beneath the mask layer and next to the
10 first pad layer; and
11 a mask liner formed on the sidewall of the mask layer and filled in the cavity,
12 wherein the mask liner has a width of 0 Å to 50 Å from the sidewall of the mask
13 layer.

1 10. The semiconductor structure as claimed in claim 9, wherein the mask liner
2 is a nitride.
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1 11. A method for fabricating a field oxide on a semiconductor substrate,
2 comprising the steps of:
3 (a) successively forming a first pad oxide layer and a first mask layer;
4 (b) forming an opening in the first mask layer to define a region for forming
5 the field oxide;
6 (c) removing the first pad layer exposed by the opening to form a cavity;
7 (d) forming a second pad layer having a smaller thickness than the first pad
8 layer on the semiconductor substrate not covered by the first pad layer;
9 (e) conformably forming a second mask layer on the semiconductor substrate
10 and the first mask layer to fill the mask portion into the cavity;

11 (f) isotropically etching the second mask layer to leave a mask filler in the
12 cavity; and

1 (g) carrying out thermal oxidation to form the field oxide in the opening.

1 12. The method as claimed in claim 11, wherein step (c) is conducted by wet
2 etching.

1 13. The method as claimed in claim 11, wherein step (d) is conducted by
2 thermal oxidation.

1 14. The method as claimed in claim 11, wherein step (f) is conducted by
2 isotropic RIE using plasma of a fluorine-containing gas as an etching reactive gas.

1 15. The method as claimed in claim 14, wherein step (f) is conducted by
2 isotropic RIE using plasma of nitrogen fluoride (NF₃), SF₆, or CF₄ as an etching
3 reactive gas.

1 16. The method as claimed in claim 15, wherein step (f) is conducted by
2 isotropic RIE using plasma of SF₆ as an etching reactive gas.

1 17. A method for fabricating a field oxide on a semiconductor substrate,
2 comprising the steps of:

3 (a) successively forming a first pad oxide layer and a first mask layer;

4 (b) forming an opening in the first mask layer to define a region for forming
5 the field oxide;

6 (c) removing the first pad layer exposed by the opening to form a cavity;

7 (d) forming a second pad layer having a smaller thickness than the first pad
8 layer on the semiconductor substrate not covered by the first pad layer;

9 (e) conformably forming a second mask layer on the semiconductor substrate
10 and the first mask layer to fill the mask portion into the cavity;

11 (f) isotropically etching the second mask layer to leave a mask liner on the
12 sidewall of the first mask layer and in the cavity, wherein the mask liner has a width
13 of 0 Å to 50 Å from the sidewall of the first mask layer; and

14 (g) carrying out thermal oxidation to form the field oxide in the opening.